Minimally dissipative multi-bit logical operations

Jérémie Klinger[1], Grant Rotskoff[2]
[1]LPENS, Paris, France, [2]Stanford University, Stanford, USA

Modern computing architectures are vastly more energy-dissipative than fundamental thermodynamic limits suggest, motivating the search for principled approaches to low-dissipation logical operations. We formulate multi-bit logical gates (bit erasure, NAND) as optimal transport problems, extending beyond classical one-dimensional bit erasure to scenarios where existing methods fail. Using entropically regularized unbalanced optimal transport, we derive tractable solutions and establish general energy-speed-accuracy trade-offs that demonstrate that faster, more accurate operations necessarily dissipate more energy. Furthermore, we demonstrate that the Landauer limits cannot be trivially overcome in higher dimensional geometries. We develop practical algorithms combining optimal transport with generative modeling techniques to construct dynamical controllers that follow Wasserstein geodesics. These protocols achieve near-optimal dissipation and can, in principle, be implemented in realistic experimentally set-ups. The framework bridges fundamental thermodynamic limits with scalable computational design for energy-efficient information processing.